#5A/8-8-03
V. Jones

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Hilliges, K.

SERIAL No. Unassigned EXAMINER: Unassigned

FILED: Herewith GROUP NO.: Unassigned

TITLE: INTEGRATED CIRCUIT TESTER WITH MULTI-PORT TESTING FUNCTIONALITY

Attorney Docket No.: US 20-00-3638

Assistant Commissioner For Patents
Washington, D.C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 5/30/01 (Date of Deposit)

Paul O. Greeley
Name

Paul D. Greeley
Signature

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the application as set forth below.

In The Abstract of the Disclosure

Please amend the Abstract of the Disclosure as follows:

Automated test equipment (ATE) includes a tester-per-pin architecture with a number of individual decentralized per-pin testing units, wherein each per-pin testing unit is adapted for testing a respective DUT-pin of a device under test (DUT) by emitting stimulus response signals to the respective DUT-pin and/or receiving stimulus response signals from the respective DUT-pin. Testing the DUT includes defining for a testing sequence the DUT into one or more DUT-cores representing one or more functional units of the DUT and covering one or more DUT-pins of the DUT, and assigning during the testing sequence one or more of the per-pin testing units to one or more ATE-ports, whereby each ATE-port comprises one or more of the per-pin testing units and represents an independent functional testing unit for testing one or more of the DUT-cores during the testing sequence.

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